

Static CMOS Design

Introduction to Circuit Design

– Lecture Series by Intel



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Lecture Series

Introduction to CMOS

APR 30th

Static CMOS Design

APR 30th

CMOS Logic Styles

MAY 21st

Sequentials & Memory

MAY 21st



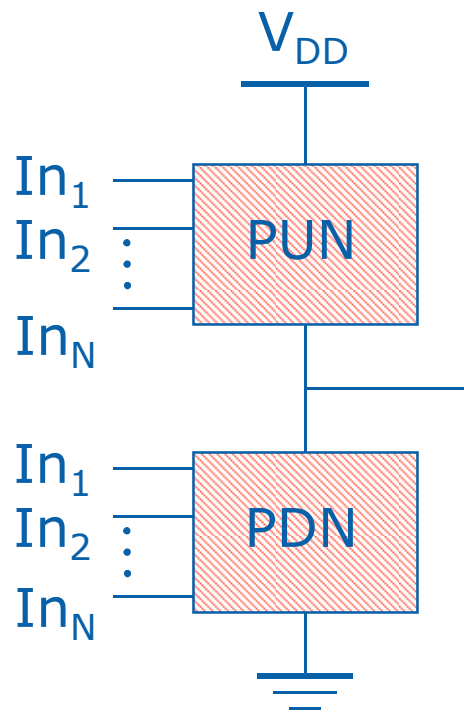
Static CMOS Design

What will we learn?

- ❑ Static CMOS Construction
- ❑ Steady State Response and Noise
- ❑ Transient Response
- ❑ Power components
- ❑ Advantages of Static CMOS



Static Complementary MOS



PMOS transistors only

pull-up: make a connection from V_{DD} to F when $F(In_1, In_2, \dots, In_N) = 1$

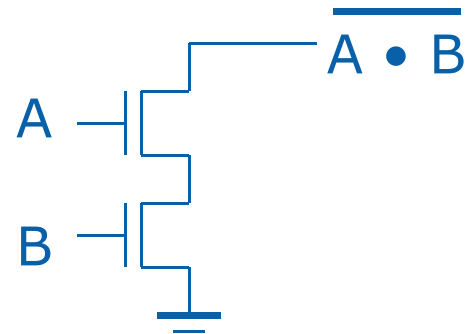
$F(In_1, In_2, \dots, In_N)$

pull-down: make a connection from F to GND when $F(In_1, In_2, \dots, In_N) = 0$

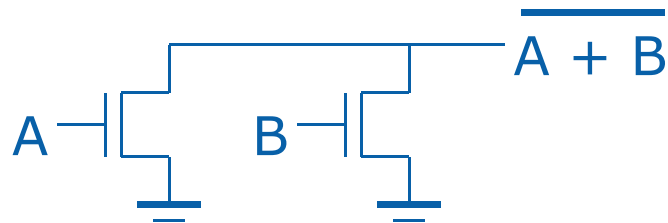
NMOS transistors only

Construction of PDN

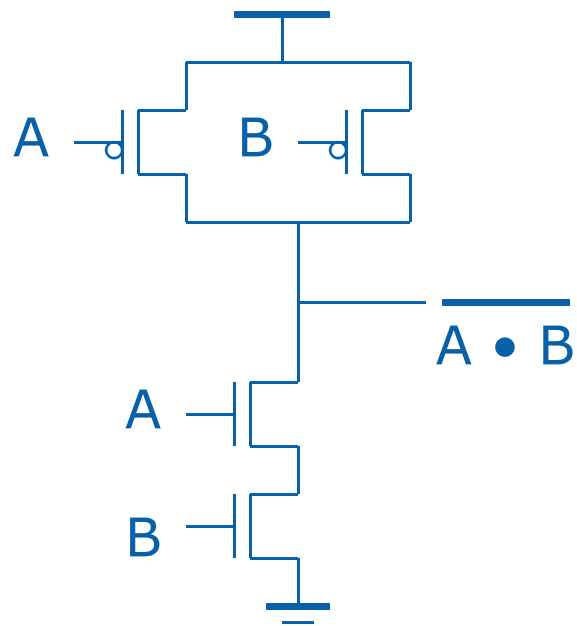
NMOS devices in **series** implement a NAND function



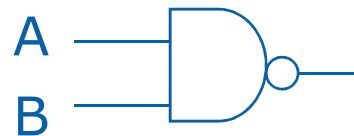
NMOS devices in **parallel** implement a NOR function



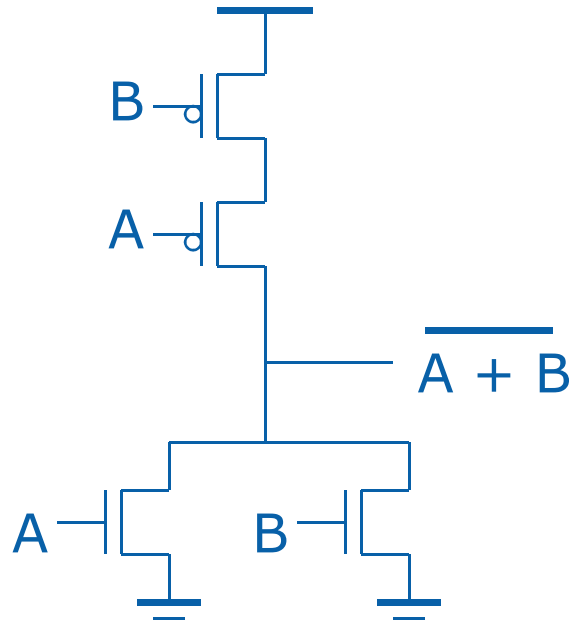
CMOS NAND



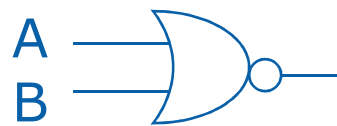
A	B	F
0	0	1
0	1	1
1	0	1
1	1	0



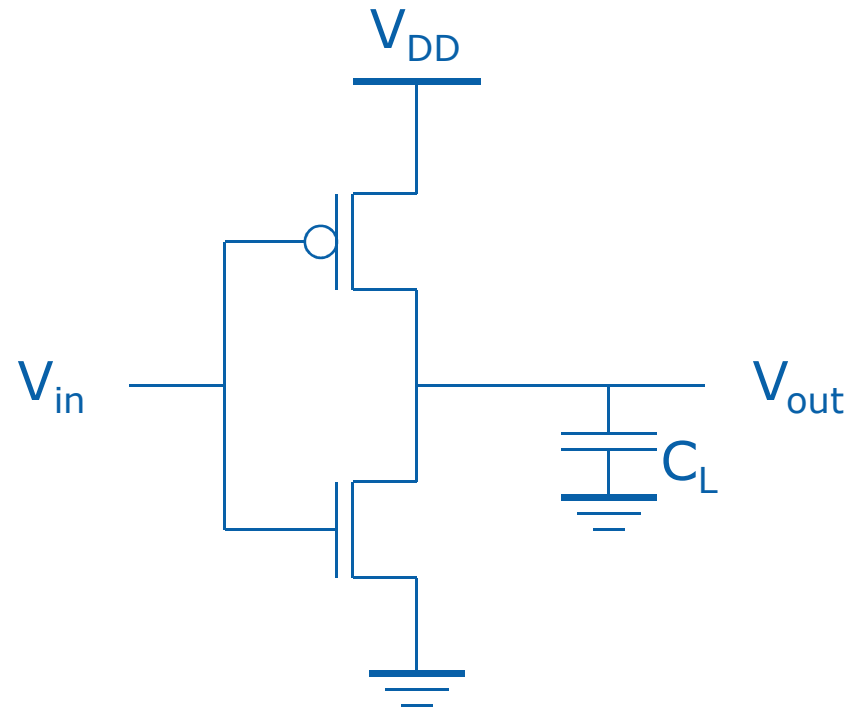
CMOS NOR



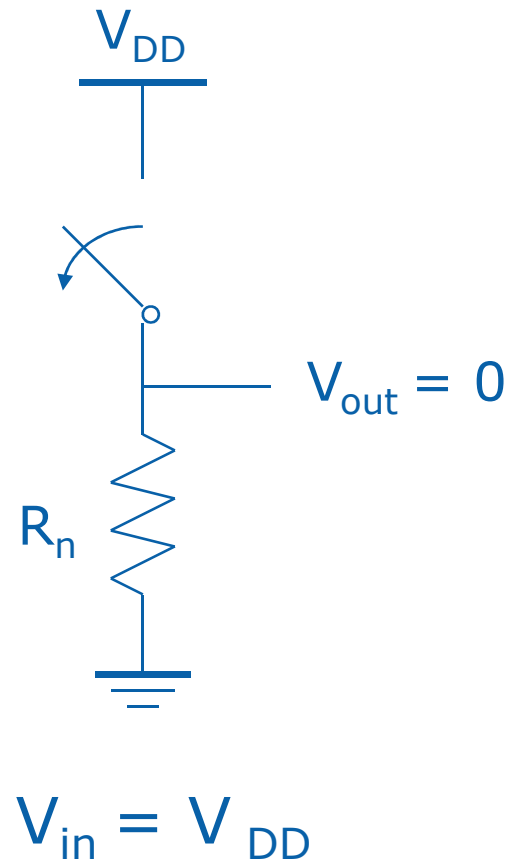
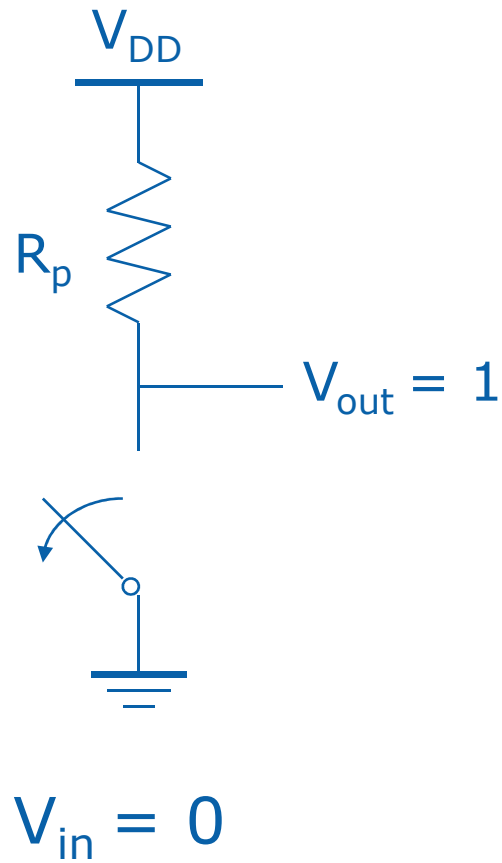
A	B	F
0	0	1
0	1	0
1	0	0
1	1	0



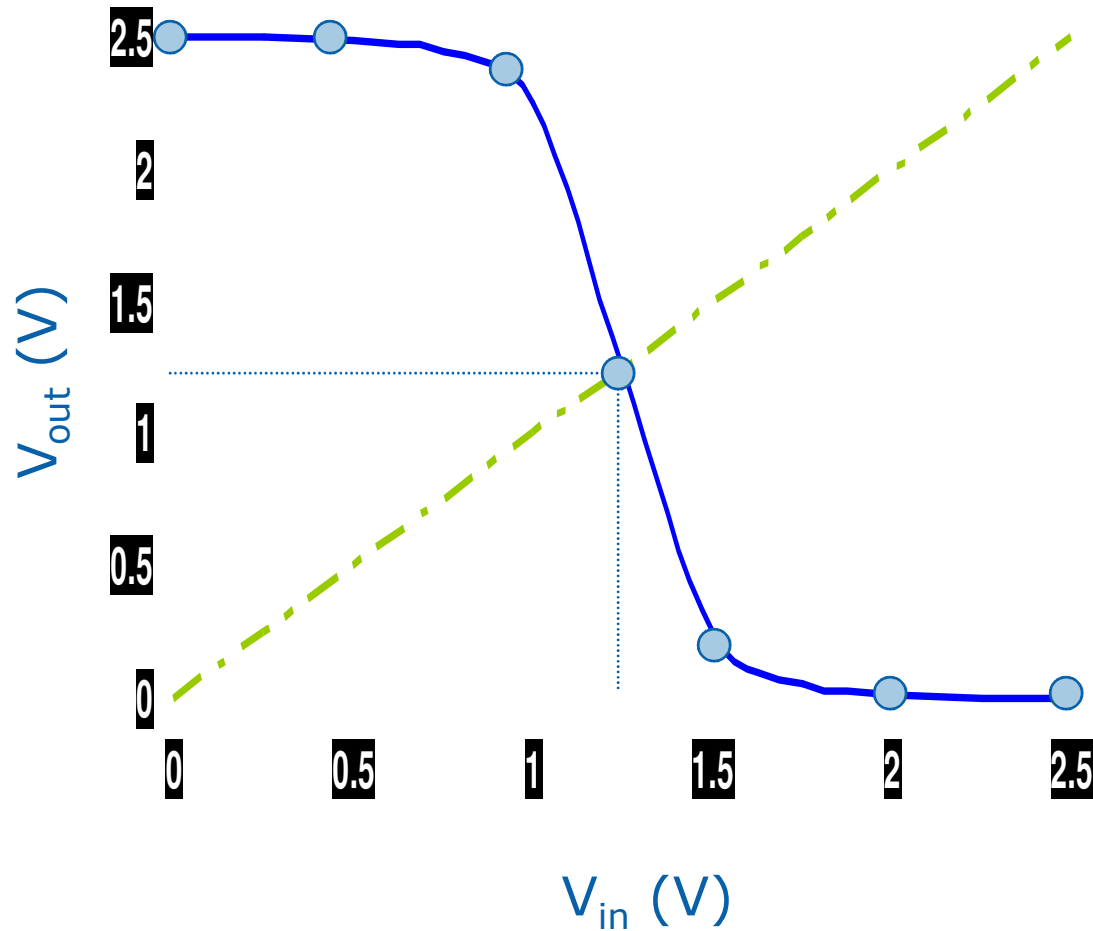
CMOS Inverter



Steady State Response



Steady State Response



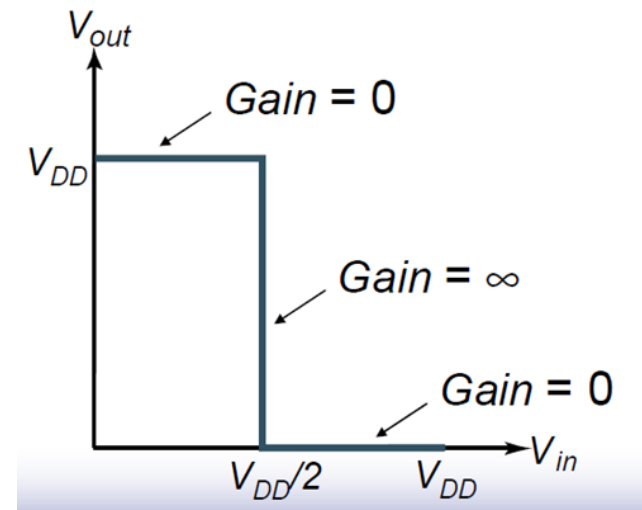
Noise in Digital Systems

- Digital systems need to work in the presence of analog “noise”
- Digital systems functions by mapping certain discrete values to analog levels
- Digital systems should have the ability to reject noise i.e., for small input noise – the output noise has to be lesser than input noise
- This ability of design is termed as noise rejection

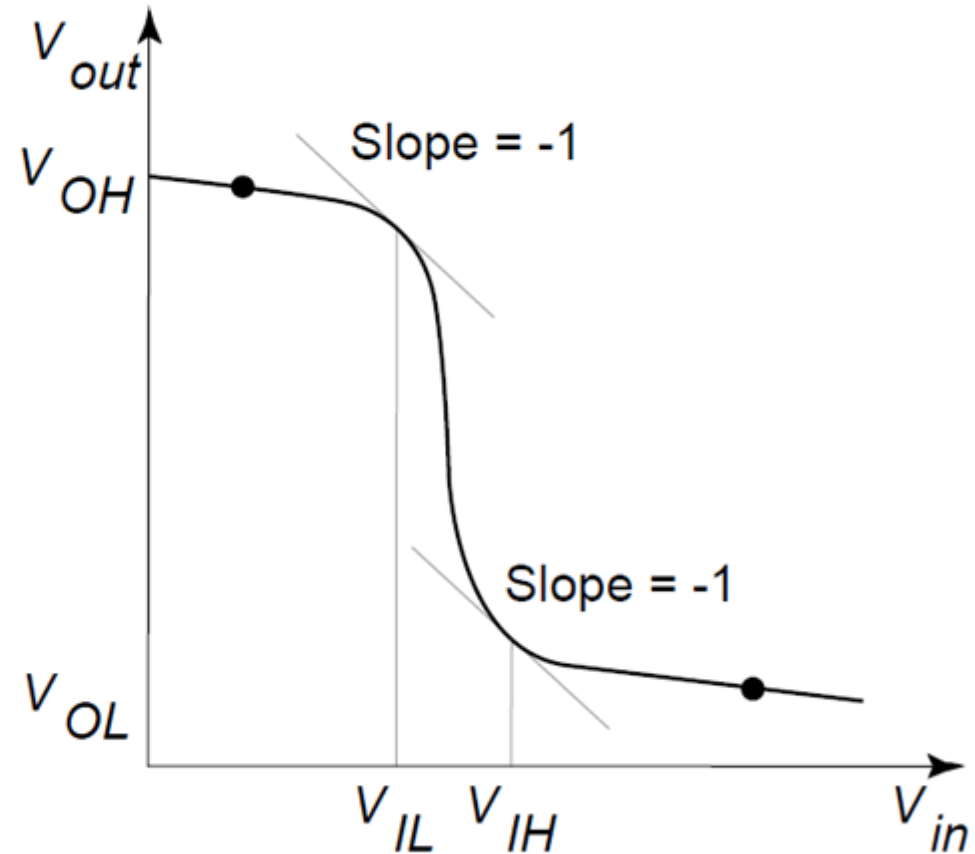
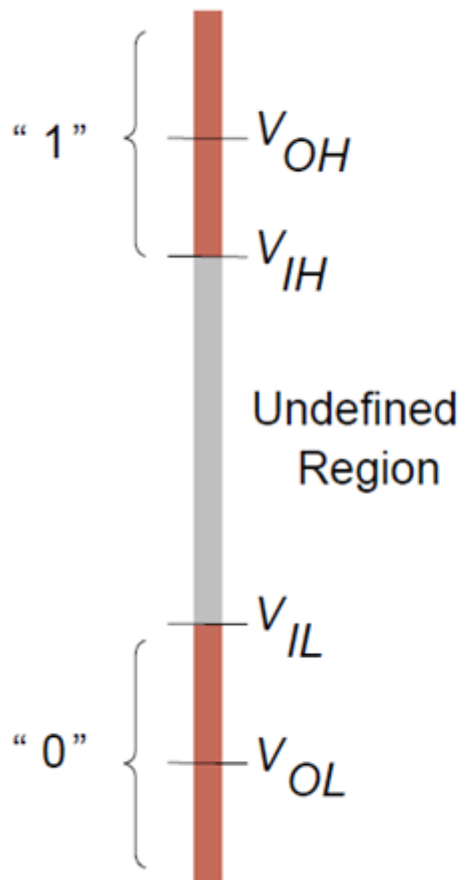


Noise Rejection

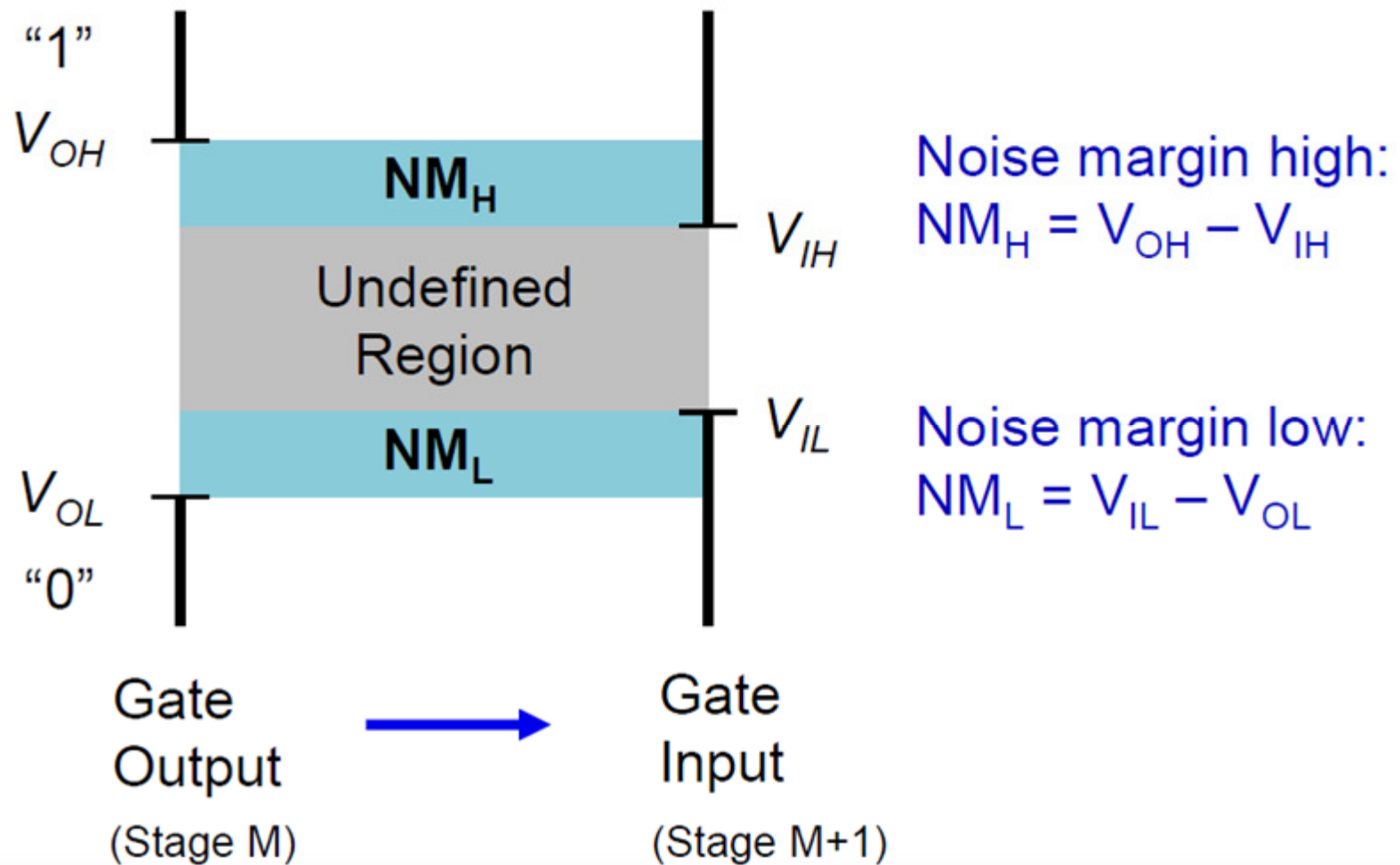
- How do we check if the gate rejects noise?
 - Observe the DC characteristics (VTC curve)
 - See what happens when input is not exactly vcc or 0
- For an ideal digital gate:
 - Noise needs to be greater than $v_{cc}/2$ to have any impact on the output



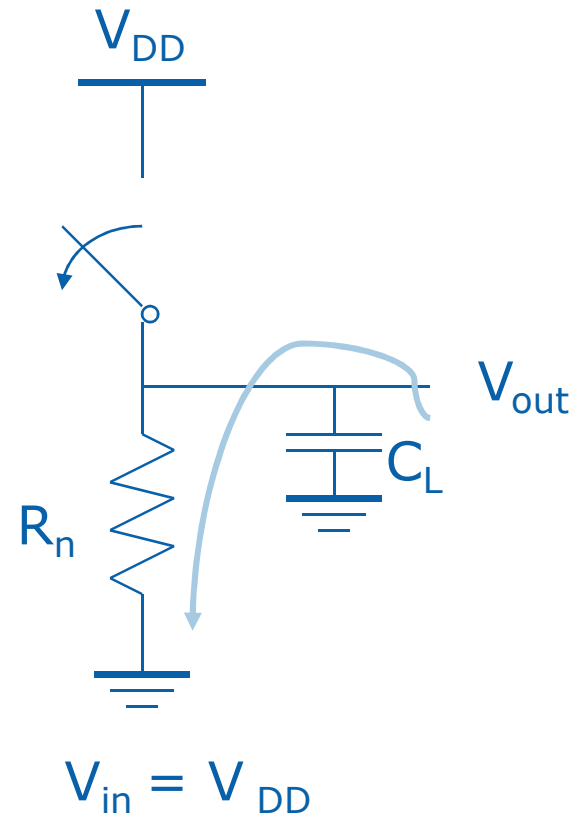
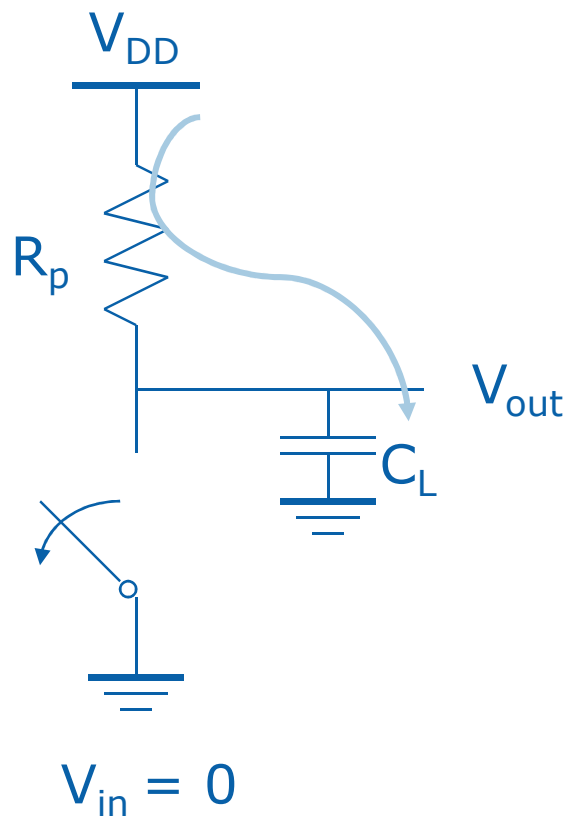
Voltage Mapping



Noise Margins



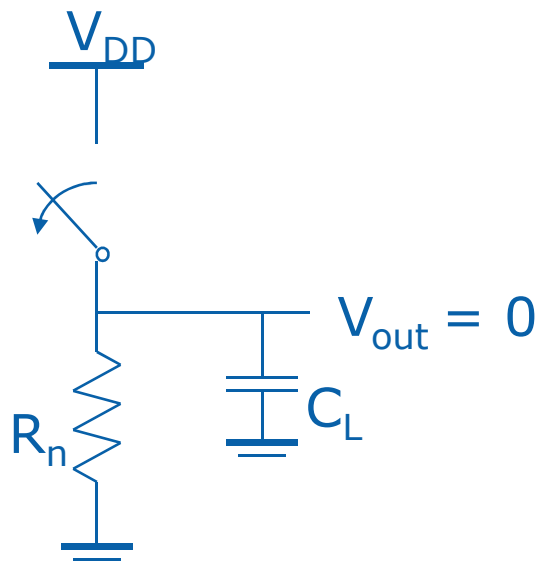
Dynamic Behavior



- Gate response time is determined by the time to charge C_L through R_p (discharge C_L through R_n)

Inverter Propagation Delay

Propagation delay is proportional to the time-constant of the network formed by the pull-down resistor and the load capacitance



$$V_{in} = V_{DD}$$

$$t_{pHL} = f(R_n, C_L)$$

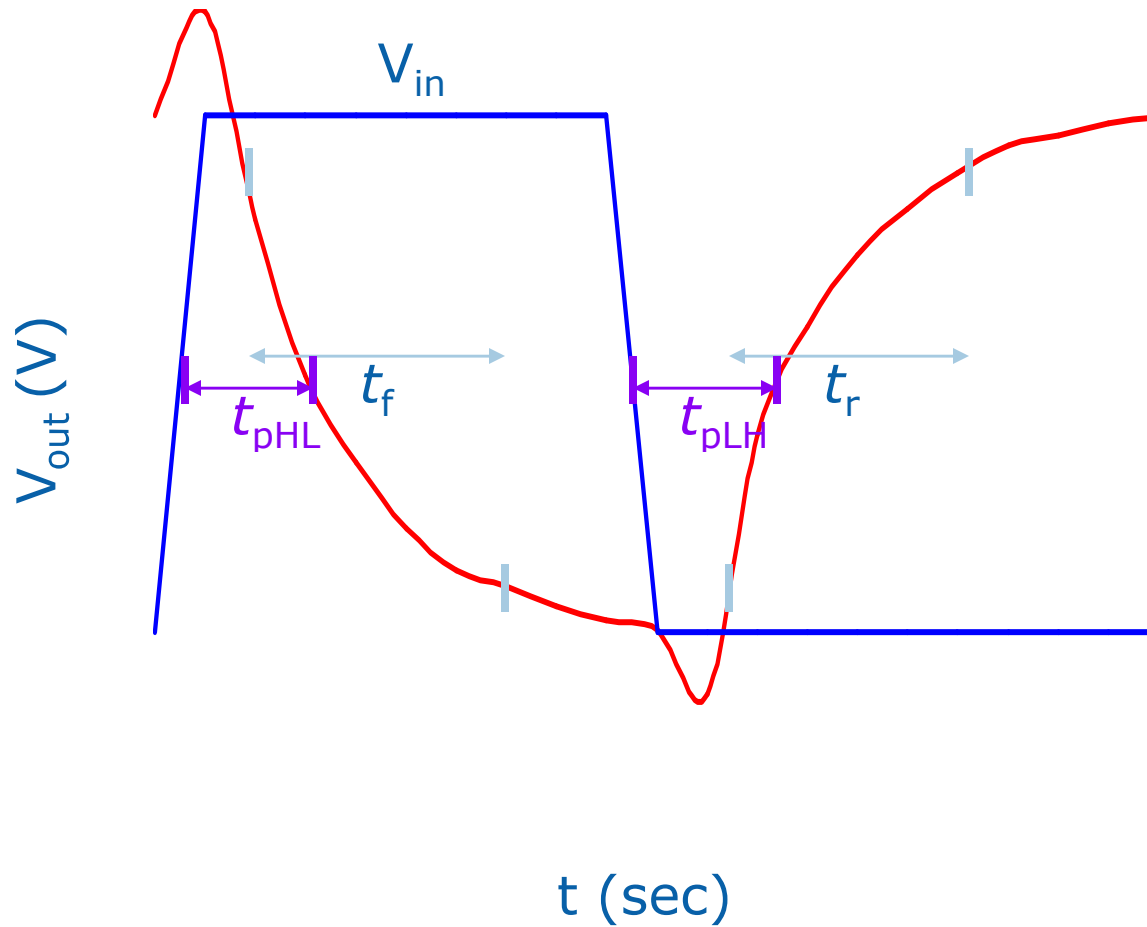
$$t_{pHL} = 0.69 R_{eqn} C_L$$

$$t_{pLH} = 0.69 R_{eqp} C_L$$

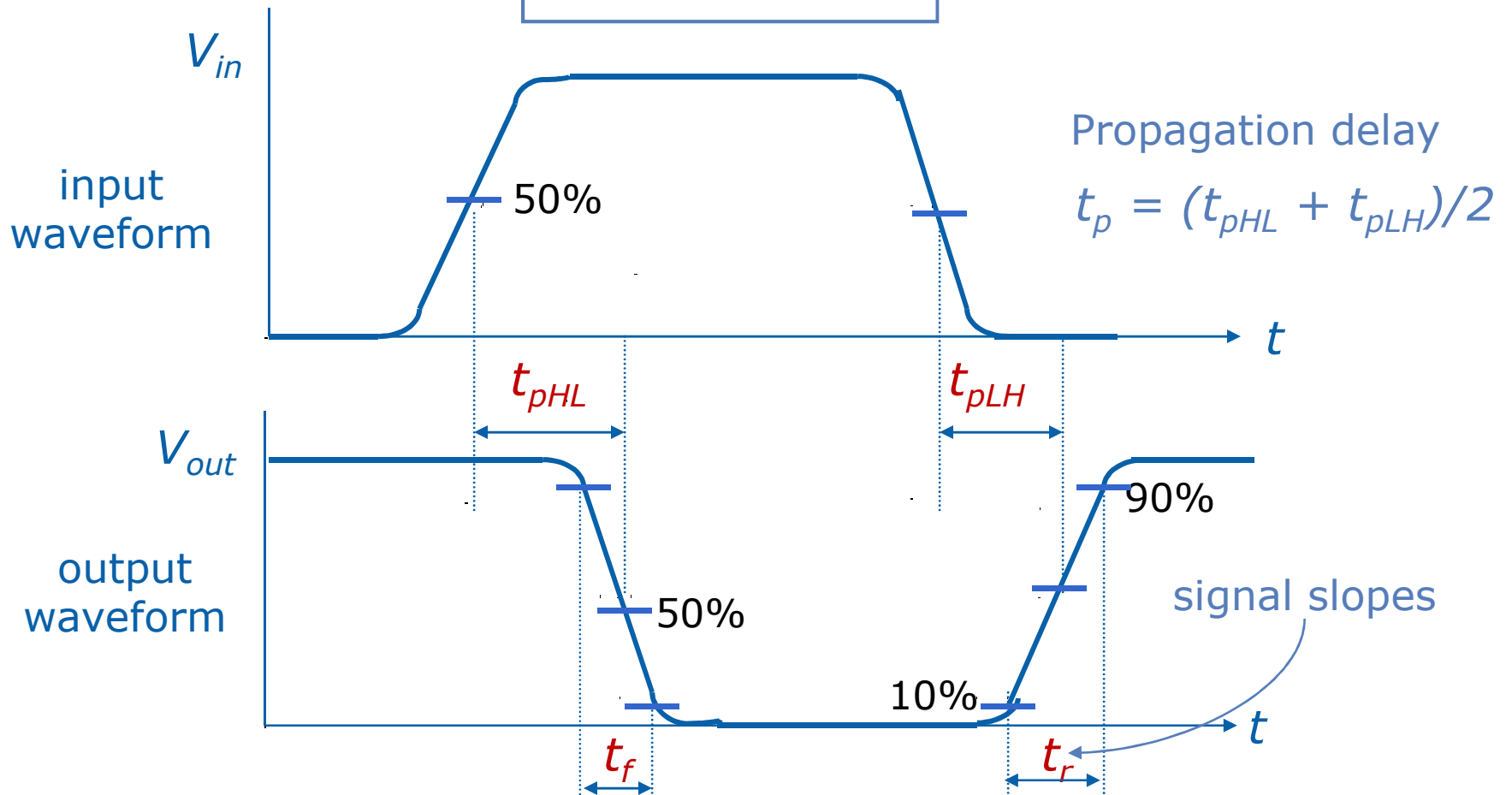
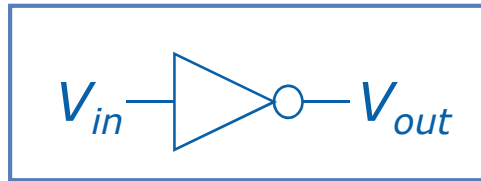
$$t_p = (t_{pHL} + t_{pLH})/2 = 0.69 C_L (R_{eqn} + R_{eqp})/2$$

To equalize rise and fall times make the on-resistance of the NMOS and PMOS approximately equal.

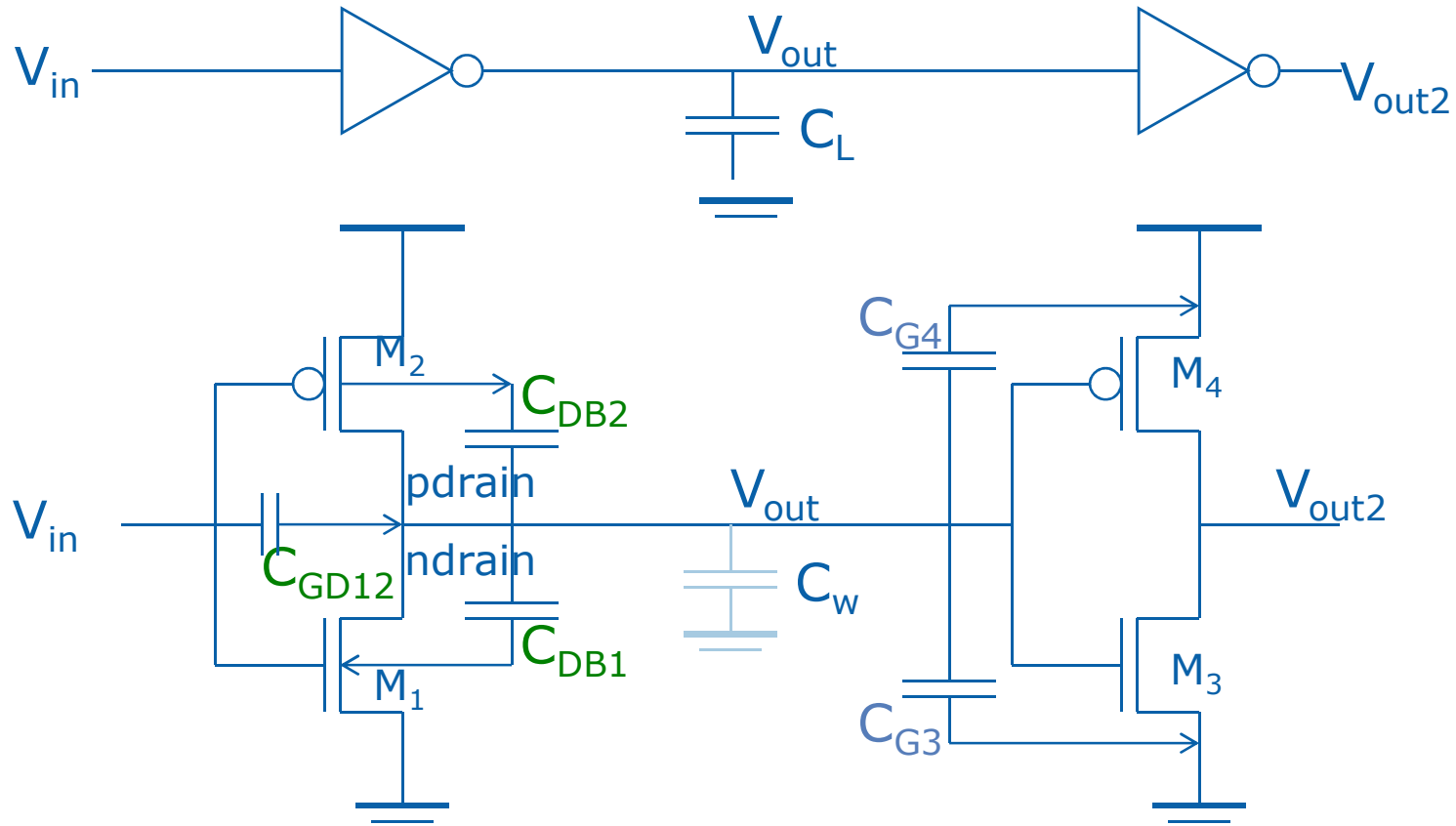
Transient Response



Delay Definitions



Sources of Capacitance

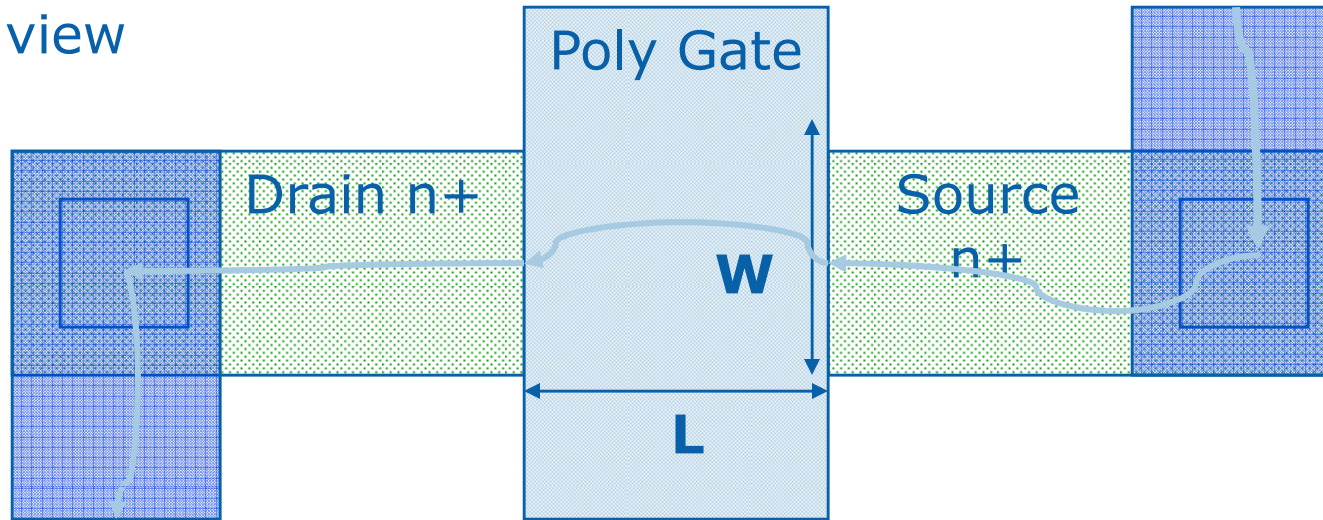


intrinsic MOS transistor capacitances

extrinsic MOS transistor (fanout) capacitances

Sources of Resistance

Top view



MOS structure resistance - R_{on}

Source and drain resistance

Contact (via) resistance

Wiring resistance

Design for Performance

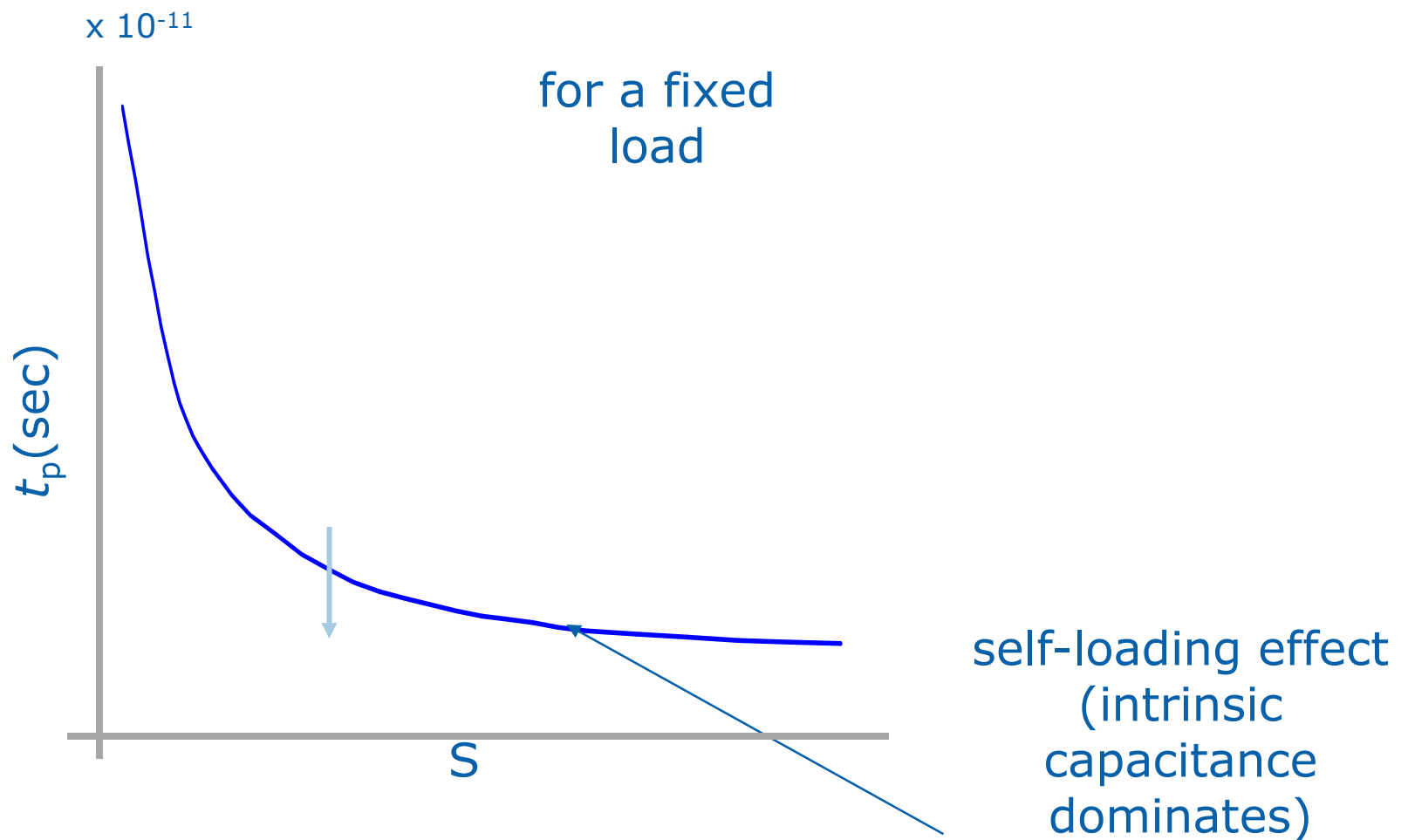
- Increase W/L ratio of the transistor
 - the most powerful and effective performance optimization tool in the hands of the designer
 - watch out for self-loading!

- Reduce C_L
 - keep drain diffusions small
 - limit interconnect capacitance
 - limit fan-out

- Increase V_{DD}
 - trade-off energy for performance
 - increasing V_{DD} above a certain level yields minimal improvements
 - reliability concerns enforce a firm upper bound on V_{DD}



Sizing Impacts on Delay

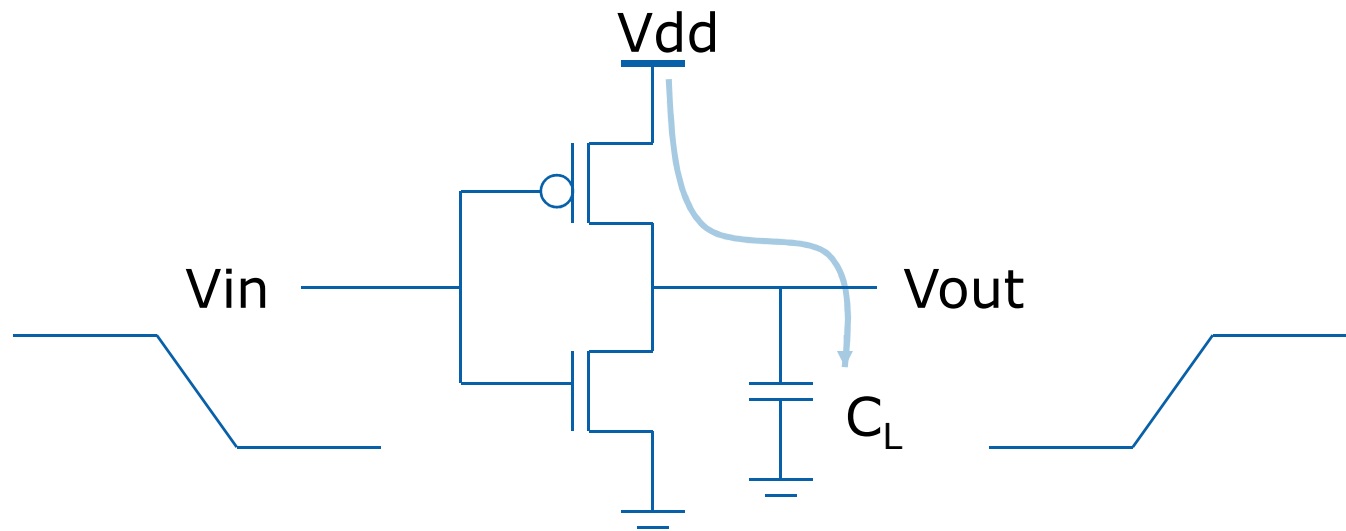


CMOS Power Equations

$$P = C_L V_{DD}^2 f + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leak}$$

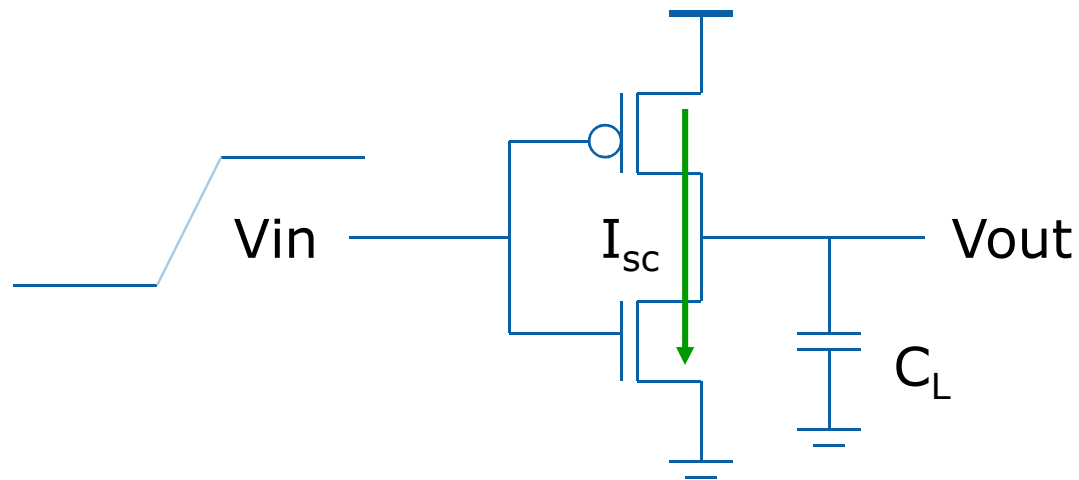
Dynamic power Short-circuit power Leakage power

Dynamic Power



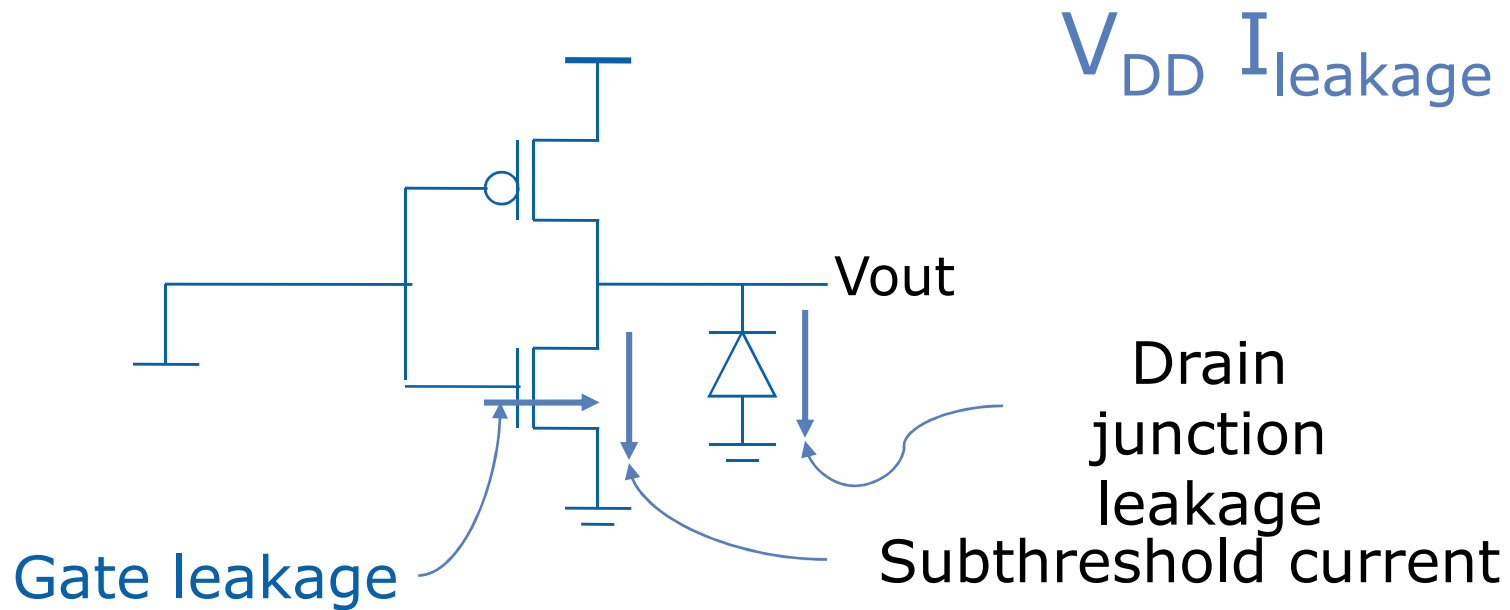
$$P_{\text{dyn}} = C_L * V_{DD}^2 * P * f$$

Short Circuit Power



Finite slope of the input signal causes a direct current path between V_{DD} and GND for a short period of time during switching when both the NMOS and PMOS transistors are conducting.

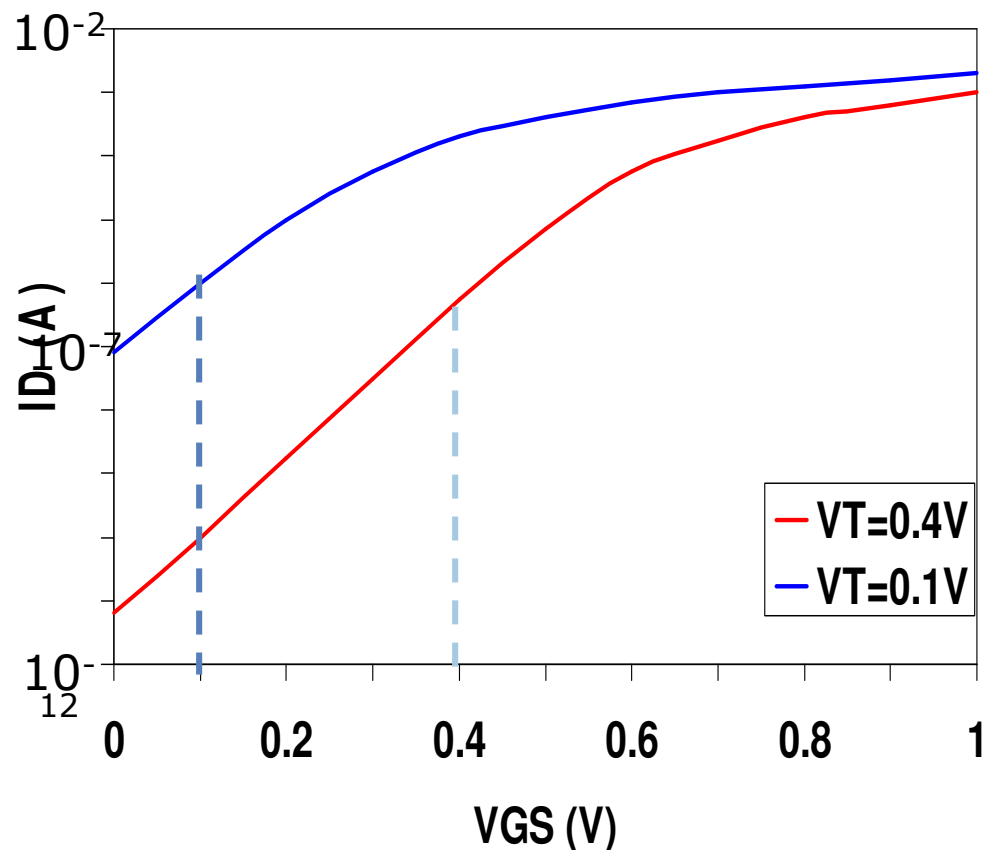
Leakage Power



Sub-threshold current is the dominant factor.

Leakage as a Function of V_T

- Continued scaling of supply voltage and threshold voltage will make subthreshold conduction a dominate component of power dissipation.



CMOS Power

$$P = C_L V_{DD}^2 f + t_{sc} V_{DD} I_{peak} f + V_{DD} I_{leak}$$

Dynamic
power
(~65% today
and decreasing
relatively)

Short-circuit
power
(~5% today
and
decreasing
absolutely)

Leakage
power
(~30% today
and
increasing)



Static CMOS Advantages

- ❑ Full rail-to-rail swing \Rightarrow high noise margins
- ❑ Low output impedance (high noise immunity)
- ❑ High input impedance
- ❑ No direct path steady-state between power and ground \Rightarrow no static power dissipation
- ❑ Ratioless
- ❑ Most widely used logic type

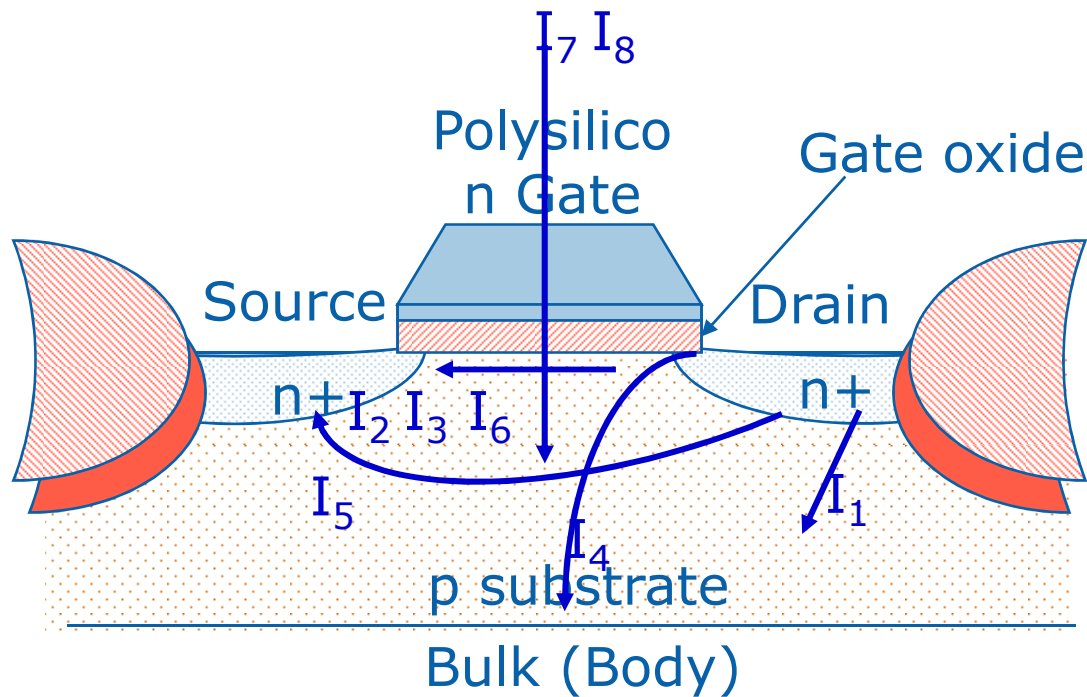


Static CMOS Design

What **did** we learn?

- ✓ Static CMOS Construction
- ✓ Steady State Response and Noise
- ✓ Transient Response
- ✓ Power components
- ✓ Advantages of Static CMOS

Leakage Current Mechanisms



- I_1 p-n junction reverse bias current (drain junction)
- I_2 weak inversion (subthreshold current)
- I_3 DIBL
- I_4 GIDL
- I_5 punchthrough
- I_6 narrow width effect
- I_7 gate oxide tunneling (gate leakage)
- I_8 hot carrier injection

Short Circuit Currents Determinates

$$E_{sc} = t_{sc} V_{DD} I_{peak} P_{0 \rightarrow 1}$$

$$P_{sc} = t_{sc} V_{DD} I_{peak} f_{0 \rightarrow 1}$$

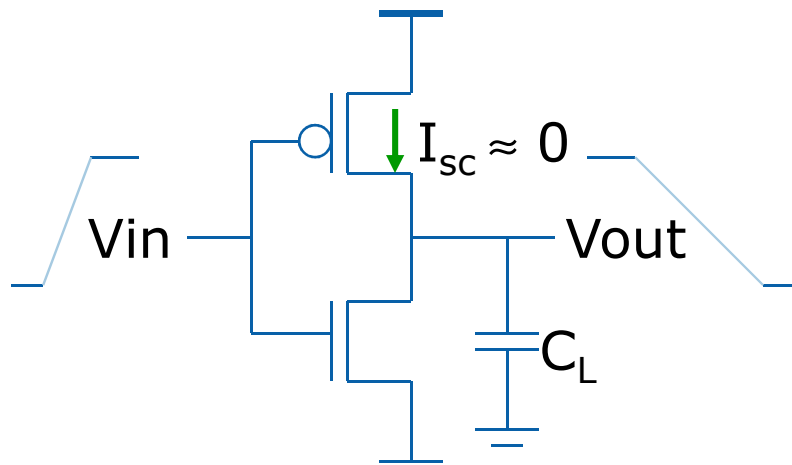
Duration and slope of the input signal, t_{sc}

I_{peak} determined by

- the saturation current of the P and N transistors which depend on their sizes, process technology, temperature, etc.
- strong function of the ratio between input and output slopes
 - a function of C_L

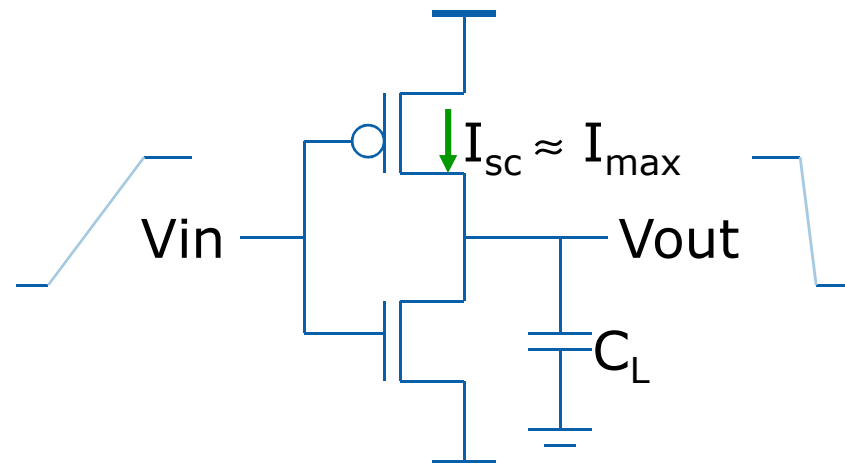


Impact of C_L on P_{sc}



Large capacitive load

Output fall time significantly larger than input rise time.



Small capacitive load

Output fall time substantially smaller than the input rise time.

Sizing

PN ratios for static CMOS should be usually chosen to optimize the total path delay.

High and low skewed sizing add design flexibility when a critical delay occurs at one edge (and not at the other).

CMOS clock buffers are sized to obtain symmetrical transitions to maintain a 50% duty cycle & equal edge rates.

Symmetrical transitions are good also for noise margins.

